IDEC Chip Design Contest

A Low Power AI Processor for face expression recognition based on k-NN and RBF

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Abstract

As the interest in an Artificial Intelligence (AI) increases, realizing the AI algorithm on a local device with low power consumption is under study. We present a low power AI processor based on k-NN and RBF algorithms. By acquiring training data once, it makes to classify the test data. We demonstrated the AI processor with an FPGA and we set up experimental environment for facial recognition to verify our chip implementation. We fabricated the AI processor with Magnachip/ Hynix 0.35um CMOS technology and it operates in 3.3V, 25MHz.

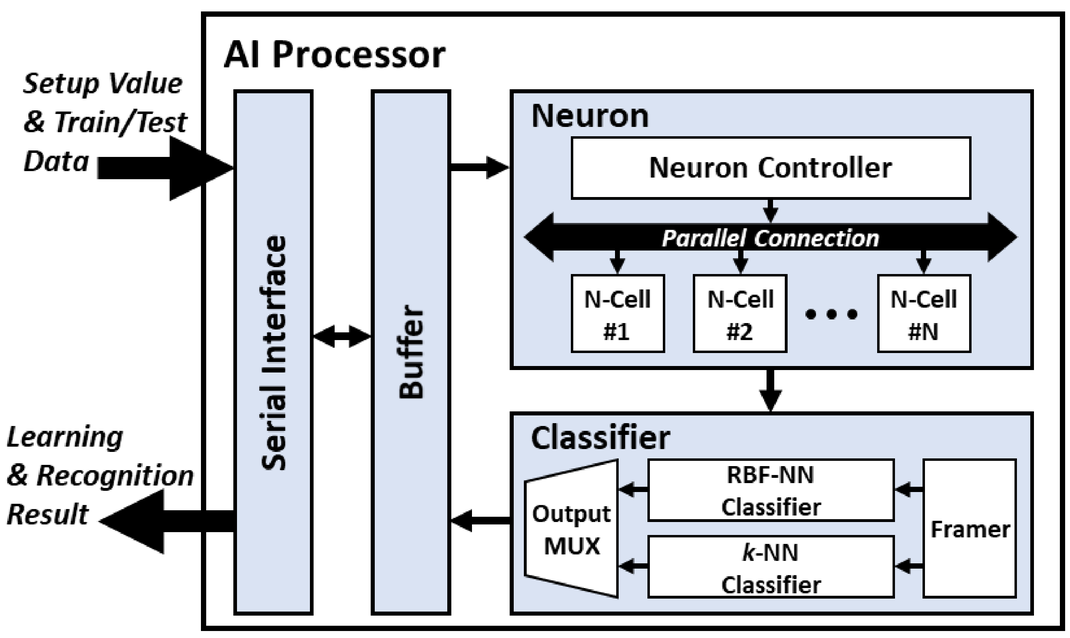
AI Processor

Operation flow

In order to operate the AI processor, it receives data type. It includes the information of algorithm selection to process and the selection of training or test data. Depending on the data type information, training data or test data is transmitted to a same module but works different. When the training data is transmitted, the AI processor stores the feature data of training data. When the test data is transmitted, it is compared with each trained data and performs the classification. With the result of the classification, the test data gets the classified label.

Architecture

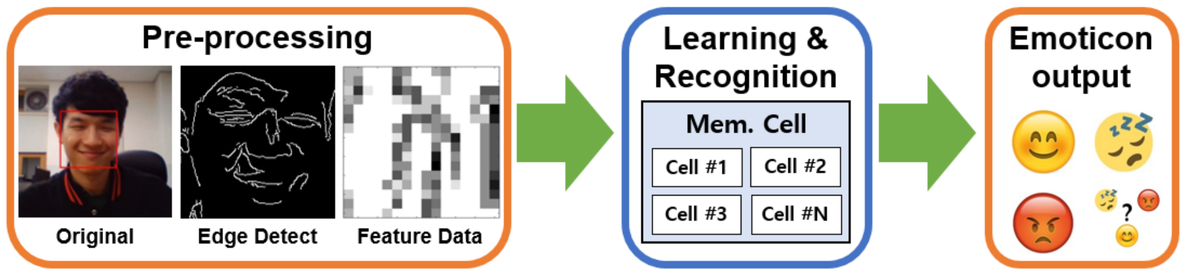
The AI processor consists of serial interface, buffer, neuron, and classifier module. To perform learning or recognition, training or test dataset are transmitted to the neuron module through the serial interface and the buffer. Then the neuron controller starts learning or recognition process. In learning process, the neuron controller points a target N-cell and the N-cell stores the dataset and category. In recognition process, incoming dataset is broadcasted to all learned N-cells. Each N-cell calculates the distance of incoming data compared to the trained data. The accumulated values are delivered to the framer in a classifier module. Then classification is conducted with the designated the classifier module between k-NN or RBF. The recognition result is informed to the external system through the buffer and the serial interface.



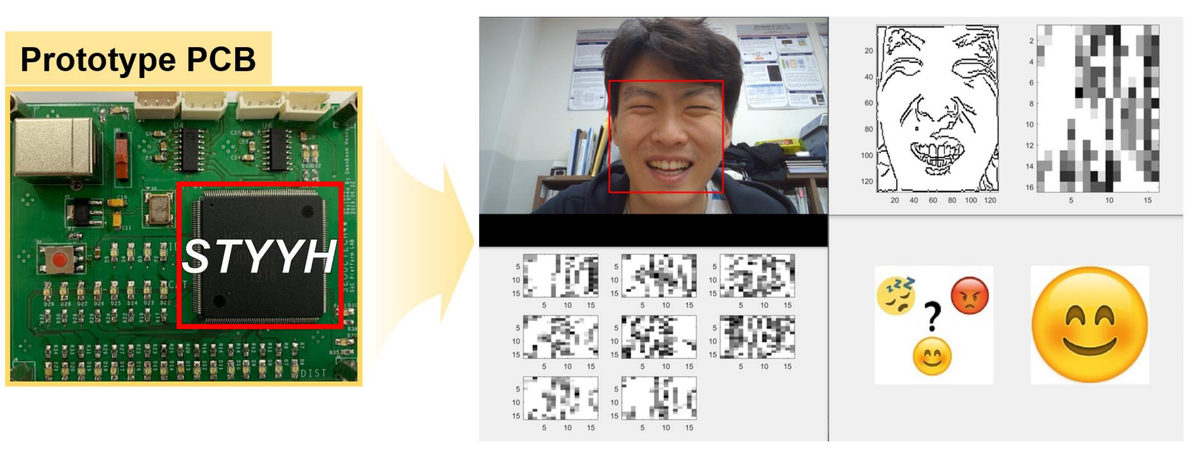
[Architecture of AI Processor]

Verification

In order to verify our design, we set up experimental environment using FPGA and a host PC with a camera. We demonstrated the AI processor with an FPGA and it is connected to the host PC that is used for external system. The camera takes a face image and the image is pre-processed to reduce size of training or test data. The processed dataset is delivered to the AI processor through a serial port. To demonstrate the recognition, we used prepared training dataset for smile, angry, and snooze facial expressions. The AI processor informs the result of facial recognition based on these three kind of trained data. We designed a prototype PCB including our chip to verify the functionality of our chip.



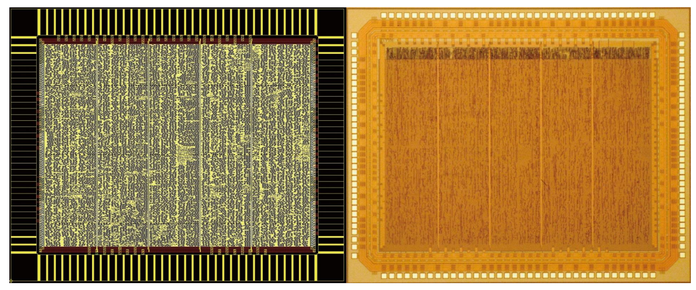
[Procedure of face expression recognition]



[Verification prototype and result]

Chip Implementation

Chip specifications	
Technology	0.35um CMOS
Supply Voltage	3.3V
Chip Size	5×4mm^2
Max. Frequency	25MHz
Gate Counts	157K @ 25MHz



[Chip layout & photograph]

Acknowledgement

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